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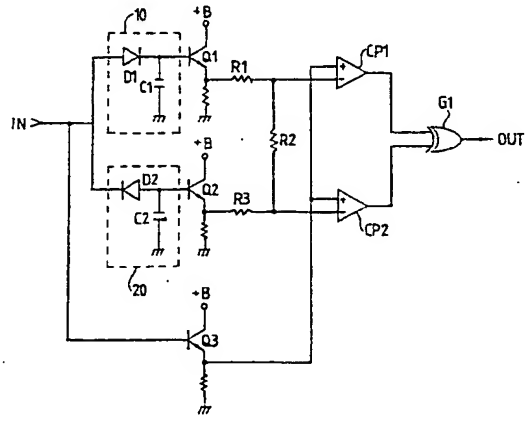
(54) Duobinary to binary decoder.

(57) Disclosed is a decoder for converting a duobinary signal into a binary signal for use in a receiver of a multiplexed analog component signal which comprises a pushpull circuit outputting an inverting and non-inverting signals of a received duobinary signal, an upper peak detector for detecting an upper peak value from the non-inverting signal, a lower peak detector for detecting an upper peak value from the inverting signal, re-inverting the upper peak value, and finally outputting a lower peak value of the received duobinary signal, A DC level regulator for stably maintaining the DC level of the received duobinary signal, and a comparison operation portion in which an upper level and a lower level are set using the outputs of the upper and lower peak detectors, and the output of the DC level regulator is data-sliced according to the upper and lower levels, thereby logically operating and outputting the result. Accordingly, when the received duobinary signal is converted into the corresponding binary signal, more stable data is obtained.

FIG. 1 (PRIOR ART)



EP 0 551 858 A2

BACKGROUND OF THE INVENTION

The present invention relates to a multiplexed analog component (hereinafter referred to as MAC) signal receiver, and more particularly to a duobinary to binary decoder for converting duobinary data of a MAC signal into binary data.

Generally, a TV or VCR adopting a MAC signal processing method includes a MAC signal receiver for receiving the MAC signal. The MAC signal is received as a signal of a state of duobinary data in the MAC signal receiver. For the purpose of digital-processing information included in the received signal, the duobinary data should be converted into binary data. An example of a conventional duobinary to binary decoder for converting duobinary data of the MAC signal into binary data is shown in FIG.1.

In FIG.1, the conventional duobinary to binary decoder comprises an input terminal IN to which a duobinary signal of the received MAC signal is input, an upper peak detector 10 for detecting a peak value of a positive region in the input signal, a lower peak detector 20 for detecting a peak value of a negative region in the input signal, a first comparator CP1 which receives a duobinary signal as a comparison signal and an output of upper peak detector 10 as a reference voltage signal, so as to produce binary data corresponding to the positive region of the duobinary signal, a second comparator CP2 which receives the duobinary signal as a comparison signal and an output of lower peak detector 20 as a reference voltage signal, so as to produce binary data corresponding to the negative region of the duobinary signal, an exclusive-OR gate G1 which exclusive-OR-operates output data of first and second comparators CP1 and CP2 to produce binary data.

The duobinary signal input through input terminal IN is added with a certain magnitude of DC voltage (+B) in a third transistor Q3 and then the added signal is input to non-inverting terminals (+) of first and second comparators CP1 and CP2, respectively. Upper peak detector 10 and lower peak detector 20 which are connected to input terminal IN in parallel to each other detect the upper peak value and the lower peak value of the input duobinary signal, respectively. Here, upper peak detector 10 comprises a forward first diode D1 and a first capacitor C1, and lower peak detector 20 comprises a backward second diode D2 and a second capacitor C2. The upper peak value detected in upper peak detector 10 is added with a certain DC voltage (+B) in a first transistor Q1, and the lower peak value detected in lower peak detector 20 is added with a certain DC voltage (+B) in a second transistor Q2. The emitter signals of first and second transistors Q1 and Q2 are supplied to inverting terminals (-) of first and second comparators CP1 and CP2, respectively. At this time, The respective emitter signals to be supplied to inverting terminals of first and second comparators CP1 and CP2, are voltage-divided via three resistors R1, R2 and R3. That is, the magnitude level of the signal applied in each of the inverting terminals of first and second comparators are adjusted by three resistors R1, R2 and R3. In first comparator CP1 and second comparator CP2, the signal input in inverting terminal (-) is the reference signal with which the duobinary signal input in non-inverting terminal (+) is compared. Accordingly, when the level of the duobinary signal is higher that that of the reference signal, a logic "1" is output, while when the level of the duobinary signal is lower that that of the reference signal, a logic "0" is output. Therefore, the binary data corresponding to the positive and negative regions of the duobinary signal is output from first and second comparators. The respective outputs of first and second comparators CP1 and CP2 are exclusive-OR-operated in exclusive-OR gate G1, to obtain the binary signal corresponding to the duobinary signal from output terminal OUT. Such a conventional duobinary to binary decoder is disclosed in detail in European application EP 0,339,727 A2.

However, when the above-mentioned conventional duobinary tc binary decoder detects the lower peak value which exists in the negative region of the duobinary signal, it was difficult to obtain stable detection data and to maintain the detected peak value. Also, during an actual operation of the decoder circuit, a reference DC level of the duobinary signal was lowered.

SUMMARY OF THE INVENTION

Therefore, to solve the above problems, it is an object of the present invention to provide a duobinary to binary decoder for use in an apparatus for converting a duobinary signal of a MAC signal into binary signal in which a reference DC level of the duobinary signal is constantly maintained and binary data having a stable value is output.

Thus, to accomplish one object of the present invention, there is provided a duobinary to binary decoder for use in an apparatus for converting a duobinary signal of a multiplexed analog component signal into a binary signal, the duobinary to binary decoder comprising:

a pushpull circuit for adding a predetermined DC voltage to an input duobinary signal and then outputting an inverting duobinary signal and a non-inverting duobinary signal based on the DC voltage, respectively;

an upper peak detector for receiving one of the inverting duobinary signal and the non-inverting

duobinary signal from the pushpull circuit, and detecting an upper peak value of the received signal;

a lower peak detector for receiving the other one different from the duobinary signal which is supplied to the upper peak detector among the duobinary signals output from the pushpull circuit, and detecting a lower peak value of the received signal;

a DC level regulator for receiving the inverting or non-inverting duobinary signal from the pushpull circuit and the output of the upper peak detector, and regulating and outputting the DC level of the input duobinary signal so as to be constantly maintained; and

a comparison operation portion for comparing the duobinary signal output from the DC level regulator with outputs of the upper peak detector and the lower peak detector, respectively, and outputting the binary signal corresponding to the duobinary signal by operating the comparison result.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is an examplary circuit diagram of a conventional duobinary to binary decoder.

FIG.2 is a circuit diagram of a duobinary to binary decoder according to the present invention.

FIGs.3A to 3D are waveform diagrams showing inputs and outputs of the essential parts of the circuit shown in FIG.2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described below in more detail with reference to the accompanying drawings.

In FIG.2 which shows one embodiment of a duobinary to binary decoder according to the present invention, a MAC signal of a duobianry type as shown in FIG.3A is input through input terminal IN. the input duobinary signal is first supplied to a pushpull circuit 30. Then, the duobianry signal is AC-coupled by a capacitor C3 in pushpull circuit 30. And then, the AC-coupled duobinary signal is added with a certain DC voltage by means of an external DC bias voltage source (+B) and two resistors R4 and R5. Then, the duobinary signal is applied to a base electrode of a transistor Q4. At this time, an inverting signal of the duobinary signal input to the base electrode is output from the collector electrode of transistor Q4, while the non-inverting signal thereof is output from the emitter electrode. Such a non-inverting signal output from pushpull circuit 30 is supplied to an upper peak detector 40 and a DC level regulator 50, respectively. The non-inverting signal applied to upper peak detector 40 is input to the base electrode of a transistor Q5. Then, the signal output from the emitter electrode of trnasistor Q5 is AC-coupled by a capacitor C4, and is added with a certain DC voltage by means of two resistors R9 and R10 and a DC bias voltage source (+B). Then, an upper peak value of the non-inverting signal is detected by a diode D3 and a capacitor C5. The detection signal is current-amplified by an amplifying unit composed of two transistors Q6 and Q7, to then input to the non-inverting terminal (+) of a first operational amplifier OP1. First operational amplifier OP1 plays a role of buffering the output of upper peak detector 40.

On the other hand, DC level regulator 50 AC-couples the non-inverting signal supplied from pushpull circuit 30 using a transistor Q8 and a capacitor C6, and then adds the AC-coupled signal with a bias voltage by means of three resistors R13, R14 and R15 and a transistor Q9. At this time, a collector current of transistor Q9 is varied by a voltage applied to the base electrode, in which the base voltage is controlled by the voltage signal output from first operational amplifier OP1. That is, the output voltage of first operational amplifier OP1 controls the magnitude of the DC bias voltage which is added to the AC-coupled duobinary signal. The reason why the output voltage of upper peak detector 40 is fedback to DC level regulator 50 is that when a bias voltage having a certain level is added to the AC-coupled duobinary signal, since the DC level of the original duobinary signal is varied to alter a peak value, such a variation of the DC level is compensated by being sensitively operated in correspondence to the variation, to accordingly maintain the DC level to be constant.

On the other hand, the inverting signal output from the collector electrode of transistor Q4 in pushpull circuit 30 is supplied to lower peak detector 100. Lower peak detector 100 comprises an upper peak detector 60 for detecting an upper peak value of the input signal, re-inverter 80 for again inverting the output signal of upper peak detector 60, and a reference voltage supply unit 70 for supplying a predetermined reference voltage signal to re-inverter 80. The inverting signal output from pushpull circuit 30 is input to upper peak detector 60 included in lower peak detector 100. Upper peak detector 60 detects the upper peak value of the input inverting signal and re-inverts the detected upper peak value, to thereby detect the lower peak value of the original duobinary signal. That is, lower peak detector 100 receives the duobinary signal in which the negative region is inverted into the positive region, detects the upper peak value of the inverting signal in upper peak detector 60, and re-inverts the detected upper peak value in re-inverter 80, thereby detecting the lower peak value of the duobinary signal. At this time,

reference voltage supply unit 70 including a DC bias voltage source (+B) and two transistors Q12 and Q13 generates a reference voltage signal which becomes a reference for inverting a signal which is input to inverting terminal (-) of a second operational amplifier OP2 in re-inverter 80, to then supply the reference voltage signal to the non-inverting signal (+) of second operational amplifier OP2 of re-inverter 80.

As described above, the upper peak value and the lower peak value respectively output from upper peak detector 40 and lower peak detector 100 are supplied to a third comparator CP3 and a fourth comparator CP4, respectively. The upper peak value of upper peak detector 40 is applied to the inverting terminal (-) of third comparator CP3, and the lower peak value of lower peak detector 100 is applied to the non-inverting terminal (+) of fourth comparator CP4. Also, the duobinary signal output from DC level regulator 50 is supplied to the non-inverting terminal (+) of third comparator CP3 and the inverting terminal (-) of fourth comparator CP4, respectively. Then, third comparator CP3 and fourth comparator CP4 performs data-slicing of the input duobinary signal, so that third comparator CP3 outputs the binary signal as shown in FIG.3B while fourth comparator CP4 outputs the binary signal as shown in FIG.3C. At this time, the data-slicing level is determined by means of three resistors R25, R26 and R27 connected in the input terminal of third and fourth comparators CP3 and CP4, respectively. If $R25 = R26 = R\Omega$, and $R27 = 2R\Omega$, as shown in FIG.3A, the duobinary signal is data-sliced at the level of 75% and 25% of the entire level, respectively. Then, third comparator CP3 produces a signal having a predetermined level as shown in FIG.3B with respect to the interval corresponding to not less than 75% of the level of the input duobinary signal. Fourth comparator CP4 produces a signal having a predetermined level as shown in FIG.3C with respect to the interval corresponding to not less than 25% of the level of the input duobinary signal. Such binary signals output respectively from third comparator CP3 and fourth comparator CP4, are logically operated in OR gate G2, so as to obtain a binary signal as shown in FIG.3D.

The duobinary to binary decoder according to the present invention enables other combinations of the shapes different from the embodiment shown in FIG.2. That is, in a relationship of connecting upper peak detector 40, DC level regulator 50 and lower peak detector 100 with transistor Q4 of pushpull circuit 30, it is possible to constitute another circuit in which the collector output of transistor Q4 in pushpull circuit 30 is applied to the base electrode of transistor Q10 in lower peak detector 100, and the emitter output thereof is applied to the base electrodes of transistor Q5 in upper peak detector 40 and of transistor Q8 in DC level regulator 50, respectively. Then, the inverting signal output from pushpull circuit 30 is input upper peak detector 40 and DC level regulator 50, while the non-inverting signal is input to lower peak detector 100. By doing so, through the same operation process as that of the above-described embodiment, the upper peak value and the lower peak value are detected, to thereby obtain the corresponding binary signal.

As described above, the duobinary to binary decoder according to the present invention can obtain more stable data in detecting the lower peak value of the negative region in the duobinary signal, and maintain the DC level of the duobinary signal constantly by feeding back the detected peak value data and regulating the DC level of the duobinary signal.

Claims

1. A duobinary to binary decoder for use in an apparatus for converting a duobinary signal of a multiplexed analog component signal into a binary signal, said duobinary to binary decoder comprising:

   a pushpull circuit for adding a predetermined DC voltage to an input duobinary signal and then outputting an inverting duobinary signal and a non-inverting duobinary signal based on the DC voltage, respectively;

   an upper peak detector for receiving one of said inverting duobinary signal and said non-inverting duobinary signal from said pushpull circuit, and detecting an upper peak value of the received signal;

   a lower peak detector for receiving the other one different from said duobinary signal which is supplied to said upper peak detector among said duobinary signals output from said pushpull circuit, and detecting a lower peak value of the received signal;

   a DC level regulator for receiving said inverting or non-inverting duobinary signal from said pushpull circuit and the output of said upper peak detector, and regulating and outputting the DC level of the input duobinary signal so as to be constantly maintained; and

   a comparison operation portion for comparing the duobinary signal output from said DC level regulator with outputs of said upper peak detector and said lower peak detector, respectively, and outputting the binary signal corresponding to said duobinary signal by operating the comparison result.

2. The duobinary to binary decoder according to claim 1, wherein said pushpull circuit com-

prises:

a capacitor for AC-coupling said input duobinary signal;

means for adding said predetermined DC voltage to said AC-coupled signal; and

a transistor for inverting and non-inverting said AC-coupled duobinary signal based on said predetermined DC voltage.

3. The duobinary to binary decoder according to claim 1, wherein said lower peak detector comprises:

an upper peak detector for detecting an upper peak value of the duobinary signal supplied from said pushpull circuit;

a re-inverter for inverting again the output of said upper peak detector; and

a reference voltage supply source for supplying a predetermined reference voltage to said re-inverter.

4. The duobinary to binary decoder according to claim 1, wherein said upper peak detector comprises:

a capacitor for AC-coupling the input duobinary signal;

means for adding said predetermined DC voltage to said AC-coupled signal; and

a peak value detector for detecting an upper peak value of the duobinary signal based on said DC voltage.

5. The duobinary to binary decoder according to claim 3, wherein said upper peak detector comprises:

a capacitor for AC-coupling the input duobinary signal;

means for adding said predetermined DC voltage to said AC-coupled signal; and

a peak value detector for detecting an upper peak value of the duobinary signal based on said DC voltage.

6. The duobinary to binary decoder according to claim 4, wherein said peak value detector comprises:

a diode which is connected in a forward direction with respect to said input duo binary signal; and

a capacitor which is connected to the output terminal of said diode.

7. The duobinary to binary decoder according to claim 5, wherein said peak value detector comprises:

a diode which is connected in a forward direction with respect to said input duo binary signal; and

a capacitor which is connected to the output terminal of said diode.

8. The duobinary to binary decoder according to claim 3, wherein said re-inverter is a comparator in which the output of said upper peak detector is received at the inverting terminal of said comparator, and the output of said reference voltage supply source is received at the non-inverting terminal.

9. The duobinary to binary decoder according to claim 1, wherein said DC level regulator comprises:

a capacitor for AC-coupling the duobinary signal supplied from said pushpull circuit;

means for adding said predetermined DC voltage to said AC-coupled signal; and

a transistor which is connected with said DC adding means and for receiving the output of said upper peak detector and regulating the DC value of said DC adding means based on the received signal.

10. The duobinary to binary decoder according to claim 1, wherein said comparison operation portion comprises:

means for receiving the signals respectively output from said upper and lower peak detectors, and setting predetermined upper and lower levels;

means for data-slicing the duobinary signal output from said DC level regulator according to the upper and lower levels set in said level set means; and

a logic unit for logically operating data obtained by data-slicing in the upper and lower levels, respectively in said data-slicing means to then output said binary signal.

11. The duobinnary to binary decoder according to claim 10, wherein said data-slicing means comprises:

a first comparator in which the upper level set in said level set means is applied to one input terminal, and the output of said DC level regulator is applied to the other input terminal, thereby outputting a predetermined level signal only when the output of said DC level regulator is higher than said upper level; and

a second comparator in which the lower level set in said level set means is applied to one input terminal, and the output of said DC level regulator is applied to the other input terminal, thereby outputting a predetermined level signal only when the output of said DC level regulator is lower than said lower level.

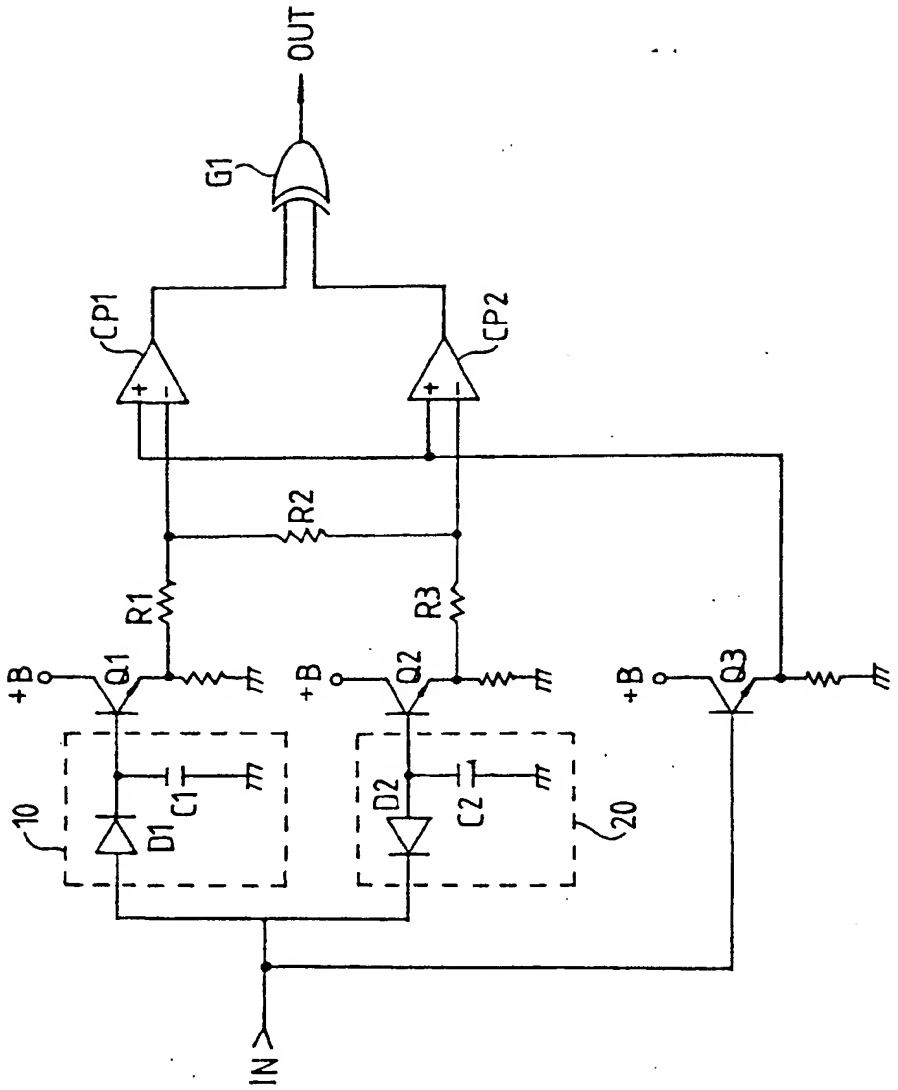
12. The duobinnary to binary decoder according to claim 10, wherein said level set means comprises:

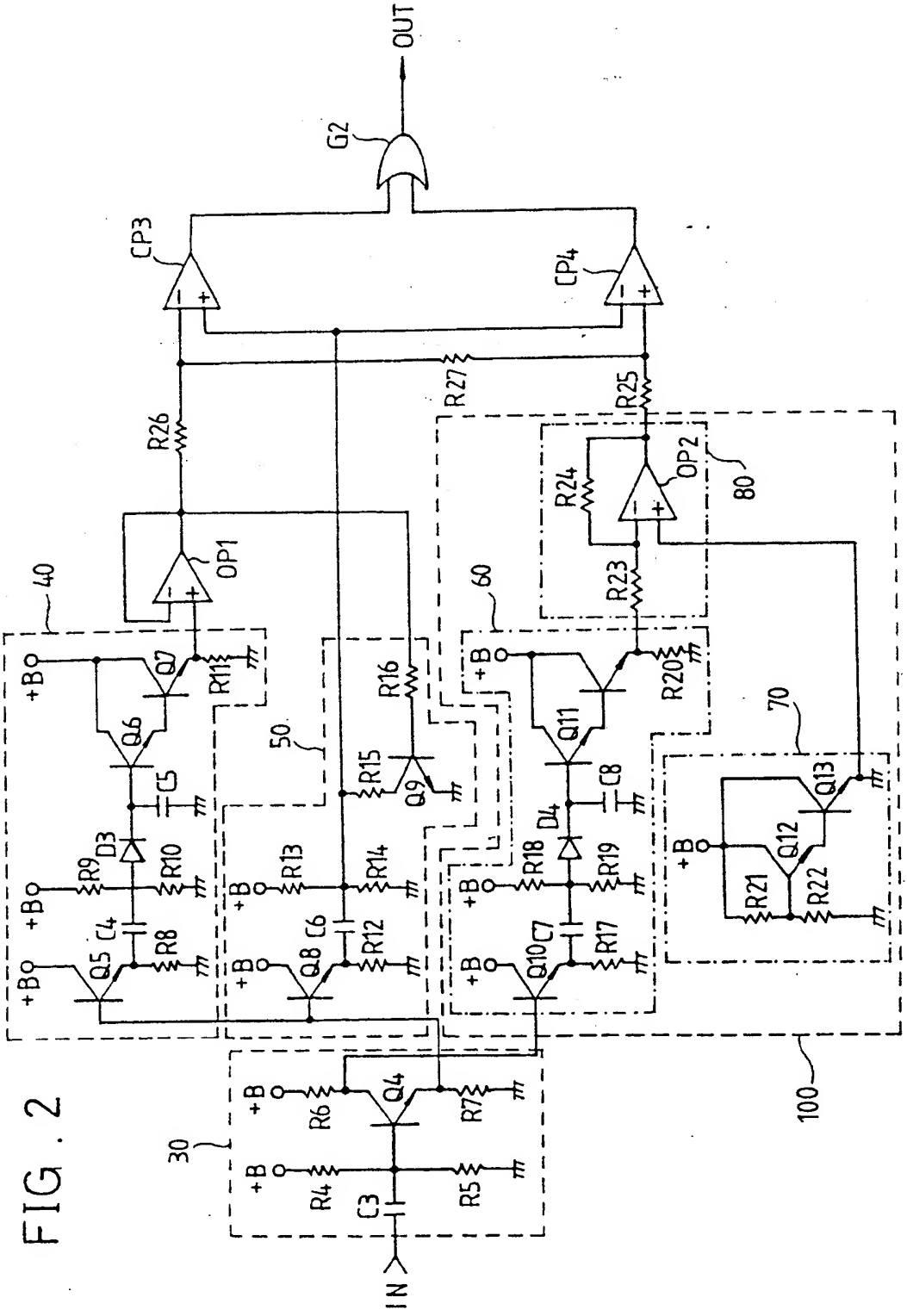
a first resistor which is connected between the output terminal of said upper peak detector and the upper level input terminal of said first comparator;

a second resistor which is connected between the output terminal of said lower peak detector and the lower level input terminal of said second comparator; and

a third resistor which is connected between said first resistor and said second resistor.

FIG. 1 (PRIOR ART)




OUT
G2
CP3
CP4
R27
R25
R26
R24
OP2
80
OP1
R23
40
60
+B
Q7
R11
R16
R20
Q6
50
Q11
70
C5
R15
Q9
C8
Q13
D3
D4
R9
R10
R13
R14
R18
R19
Q12
R21
R22
C4
C6
C7
R8
R12
R17
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Q4
R6
R7
30
R4
C3
R5
IN
100

FIG. 2

FIG.3A

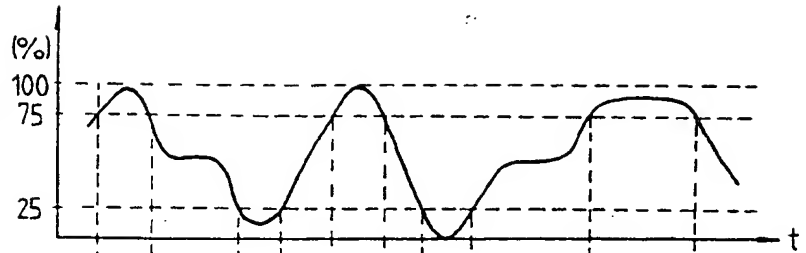


FIG.3B

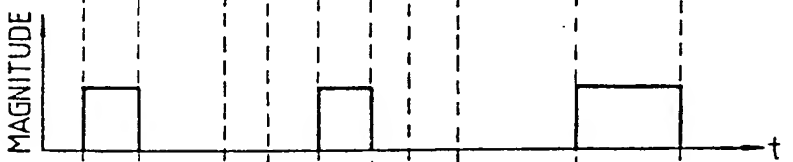


FIG.3C

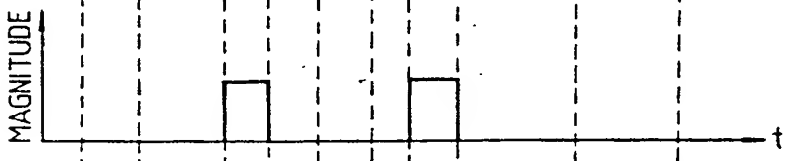
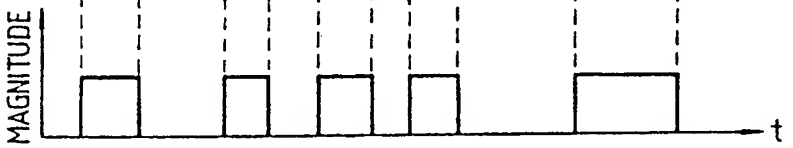


FIG.3D



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(54) **Duobinary to binary decoder.**

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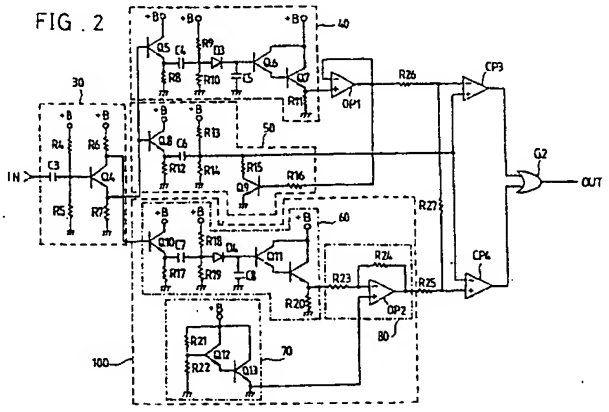
FIG. 2



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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 10 0299

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y,D A	EP-A-0 339 727 (PHILIPS) * the whole document *	1 3-7, 10-12	H04N7/00 H03K5/08 G01R19/165 H04L25/49
Y	GB-A-1 155 576 (FELTEN & GUILLEAME FERNMELDEANLAGEN) * page 2, line 92 - page 5, line 72 *	1	
A	US-A-4 007 382 (WARBERG) * figure 2 *	1-3	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H04N
H03K
G01R
H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 OCTOBER 1993	BOSCH F.M.D.

CATEGORY OF CITED DOCUMENTS

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